What is claimed is:

1. Semiconductor integrated circuit apparatus comprising: an integrated circuit main body including a plurality of MOSFETs on a semiconductor substrate;

monitor means for monitoring at least one of the drain currents of said plurality of MOSFETs; and

substrate voltage regulating means for controlling the substrate voltage of said semiconductor substrate so as to keep constant said drain current.

2. The semiconductor integrated circuit apparatus according to claims 1, further comprising a plurality of said substrate voltage regulating means.

3. The semiconductor integrated circuit apparatus according to claim 2, further comprising;

first substrate voltage regulating means for regulating a substrate potential so that the individual threshold values of the plurality of MOSFETs become uniform, and

second substrate voltage regulating means for regulating a substrate potential so that the individual drain currents of the plurality of MOSFETs are constant, and in that

the first substrate voltage current regulating means is used for substrate voltage regulation of a portion of said semiconductor integrated circuit main body in which portion

a noise margin is lower than a predetermined value, and that the second substrate voltage current regulating means is used for substrate voltage regulation of a portion of said semiconductor integrated circuit main body in which portion a noise margin is higher than the predetermined value.

4. The semiconductor integrated circuit apparatus according to claim 2, wherein the interior of said integrated circuit main body is divided into a plurality of regions, and substrate voltage regulating means for regulating the substrate voltage of a MOSFET within the region is connected to the inside or vicinity of each of the regions.

5. The semiconductor integrated circuit apparatus according to claim 2, wherein MOSFETs different in device characteristics for a substrate voltage are mounted together within said integrated circuit main body, and the same substrate voltage regulating means is connected to MOSFET groups substantially identical in said device characteristics to each other.

6. The semiconductor integrated circuit apparatus according to any one of claims 1 to 5, wherein said drain current is a drain current for an arbitrary gate voltage value in a subthreshold region or a saturated region.

7. The semiconductor integrated circuit apparatus according to any one of claims 1 to 5, wherein the gm of the transistor is kept constant by said substrate voltage regulating means.

8. The semiconductor integrated circuit apparatus according to any one if claims 1 to 7, wherein said monitor means comprises a constant current source and a monitoring MOSFET formed on the same substrate as said plurality of MOSFETs, said substrate voltage regulating means comprises comparison means for comparing the source potential of said monitoring MOSFET with a predetermined reference potential with the drain terminal of said monitoring MOSFET and the drain terminals of said plurality of MOSFETs connected to the ground potential, and that said substrate voltage regulating means feeds back the output voltage output based on the comparison result by said comparison means to the substrate voltage of said monitoring MOSFET.

9. The semiconductor integrated circuit apparatus according to claim 8, wherein said reference potential is a supply potential to the integrated circuit main body.

10. The semiconductor integrated circuit apparatus according to claim 8, wherein said substrate voltage regulating means outputs a voltage value obtained by providing, by way of limiting

means, the upper and lower limits of the output voltage output based on the comparison result of said comparison means.

11. The semiconductor integrated circuit apparatus according to claim 10, wherein said monitoring MOSFET is a p-type monitoring MOSFET, the upper limit of the output voltage value of said substrate voltage regulating means is set to a voltage equal to or above the supply potential of said integrated circuit main body and within a range where the GIDL effect does not occur in said p-type monitoring MOSFET, and the lower limit of the output voltage value of said substrate voltage regulating means is set to a voltage below the supply potential of said integrated circuit main body and within a range where said p-type monitoring MOSFET does not show the bipolar characteristics.

12. The semiconductor integrated circuit apparatus according to claim 10, wherein said monitoring MOSFET is an n-type monitoring MOSFET, the upper limit of the output voltage value of said substrate voltage regulating means is set to a voltage equal to or above the ground potential of said integrated circuit main body and within a range where said n-type monitoring MOSFET does not show the bipolar characteristics, and the lower limit of the output voltage value of said substrate voltage regulating means is set to a voltage below the ground potential of said integrated circuit main body and within a range where the GIDL

effect does not occur in said n-type monitoring MOSFET.

13. The semiconductor integrated circuit apparatus according to claim 10, wherein

the output of said limiting means is connected to voltage supply means for supplying a source voltage to said integrated circuit main body, and

said source voltage is raised when a substrate voltage is an upper limit voltage or more and said source voltage is lowered when the substrate voltage is a lower limit voltage or less.

14. The semiconductor integrated circuit apparatus according to claim 8, wherein said constant current source has a leakage current canceling MOSFET substantially identical in transistor size to said monitoring MOSFET,

when said leakage current canceling MOSFET is an n-type MOSFET, a source-drain current provided when the gate and drain of the n-type MOSFET have substantially the same potential is added, and

when said leakage current canceling MOSFET is a p-type MOSFET, a source-drain current provided when the gate and drain of the p-type MOSFET have substantially the same potential is added.

15. The semiconductor integrated circuit apparatus according

to claim 14, wherein a well region that provides the substrate of said leakage current canceling MOSFET is separated from a well region that provides the substrate of said monitoring MOSFET.

16. The semiconductor integrated circuit apparatus according to claim 8, further comprising substrate voltage regulating means for regulating a substrate potential so that the individual threshold values of the plurality of MOSFETs become uniform, and

a voltage is applied to the gate of said monitoring MOSFET as the voltage value is changed in accordance with temperature so as to provide a more gradual gradient than the temperature gradient of said threshold values formed when a voltage applied to said gate is set to be constant.

17. The semiconductor integrated circuit apparatus according to claim 8, further comprising:

frequency-voltage conversion means, wherein a signal originating from a clock supplied to the integrated circuit main body is inputted to said frequency-voltage conversion means,

the frequency of said signal is converted into a voltage by said frequency-voltage conversion means, and

said voltage is applied to the gate of a MOSFET

constituting said monitor means.

18. The semiconductor integrated circuit apparatus, having a n-well region, which become a substrate of a p-type MOSFET, and a p-well region, which is provided inside said n-well region, and become a substrate of a n-type MOSFET, according to any one of claims 1 to 17,

wherein there are provided a second p-well region and a second n-well region, and

said second p-well region is electrically connected to the substrate potential of said n-type MOSFET and said second n-well region is electrically connected to the ground potential of said n-type MOSFET.

19. The semiconductor integrated circuit apparatus, characterized by that a source and substrate are independently controlled, according to any one of claims 1 to 18, wherein a gate capacity of MOSFET is added between the source of the MOSFET and the substrate of the MOSFET.

20. The semiconductor integrated circuit apparatus, having a n-well region, which become a substrate of a p-type MOSFET, and a p-well region, which is provided inside said n-well region, and become a substrate of a n-type MOSFET, according to any one of claims 1 to 19, wherein an electric capacity value between

a p-well region that provides the substrate of an n-type MOSFET and the ground potential of said n-type MOSFET is higher than an electric capacity value between said p-well region and an n-well region that provides the substrate of a p-type MOSFET.

21. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit main body comprises a feedback buffer and the substrate voltage of the MOSFET of the feedback buffer is set by said substrate voltage regulating means.

22. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit main body comprises a memory circuit and the substrate voltage of the MOSFET of the memory circuit is set by said substrate voltage regulating means.

23. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit main body comprises an SRAM and that the substrate voltage of the MOSFET of the SRAM is set by said substrate voltage regulating means.

24. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit

main body comprises a circuit of the timing borrow system and the substrate voltage of the MOSFET of the circuit of the timing borrow system is set by said substrate voltage regulating means.

25. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit main body comprises a differential operational amplifier and the substrate voltage of the MOSFET of the differential operational amplifier is set by said substrate voltage regulating means.

26. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit main body comprises a voltage-controlled oscillator and the substrate voltage of the MOSFET of the voltage-controlled oscillator is set by said substrate voltage regulating means.

27. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit main body comprises a CMOS logic circuit and the substrate voltage of the MOSFET of the CMOS logic circuit is set by said substrate voltage regulating means.

28. The semiconductor integrated circuit apparatus according to any one of claims 1 to 20, wherein said integrated circuit

main body comprises a current-controlled oscillator and the substrate voltage of the MOSFET of the current-controlled oscillator is set by said substrate voltage regulating means.